at least two channels connecting the strapping line to a first and second end of the portion of the single wordline.

5. (Amended) A memory array, comprising:

a number of memory cells having a first source/drain region and a second source/drain region and a gate region;

a number of source lines coupled to the first source/drain region of at least one memory cell;

a number of bit lines coupled to the second source/drain region of at least one memory cell;

a number of wordlines coupled to the gate region of at least one memory cell;

a plurality of strapping lines of lower resistance than the wordlines coupled to at least one of the number of wordlines wherein the strapping lines bypass a plurality of portions of a single wordline[; and], and wherein a width of the strapping line is greater than a width of the wordlines; and

a plurality of channels connecting the plurality of strapping layers to the wordline.

8. (Twice amended) A memory device, comprising:

a number of memory cells having a first source/drain region and a second source/drain region and a gate region;

a number of source lines coupled to the first source/drain region of at least one memory cell;

a number of bit lines coupled to the second source/drain region of at least one memory cell;

an array of parallel wordlines coupled to the gate region of at least one memory cell, the array of parallel wordlines having a pitch;

a number of strapping devices which bypass portions of the wordlines in the array of parallel wordlines, each strapping device comprising:

a strapping line of lower resistance than the wordlines, wherein the strapping lines

are each located a distance from each other that is greater than the pitch[; and], and wherein a width of the strapping line is greater than a width of the wordlines; and

at least two channels connecting each strapping line to a portion of a single wordline.

15. (Twice amended) An integrated circuit comprising:

at least one memory array comprising:

a number of memory cells having a first source/drain region and a second source/drain region and a gate region;

a number of source lines coupled to the first source/drain region of at least one memory cell;

a number of bit lines coupled to the second source/drain region of at least one memory cell;

a number of wordlines coupled to the gate region of at least one memory cell;

a strapping line of lower resistance than the wordlines coupled to a single wordline wherein the strapping line bypasses a portion of the single wordline, and wherein the strapping line is spaced apart from adjacent conductive structures by a distance greater than a wordline pitch[;], and wherein a width of the strapping line is greater than a width of the wordlines;

at least two channels connecting the strapping line to a first and second end of the portion of the single wordline;

a row decoder;

a column decoder; and

a sense amplifier.

19. (Twice amended) An integrated circuit comprising:

at least one memory array comprising:

a number of memory cells having a first source/drain region and a second source/drain region and a gate region;

a number of source lines coupled to the first source/drain region of at least one memory cell;

a number of bit lines coupled to the second source/drain region of at least one memory cell;

an array of parallel wordlines coupled to the gate region of at least one memory cell, the array of parallel wordlines having a pitch;

a number of strapping devices which bypass a portion of single wordlines in the array of parallel wordlines, each strapping device comprising:

a strapping line of lower resistance than the wordlines, wherein the strapping lines are each located a distance from each other that is greater than the pitch[;], and wherein a width of the strapping line is greater than a width of the wordlines;

at least two channels connecting the strapping line to the single wordline;

a row decoder;

a column decoder; and

a sense amplifier.

26. (Twice amended) An information handling device comprising:

a processing unit;

at least one memory array comprising:

a number of memory cells having a first source/drain region and a second source/drain region and a gate region;

a number of source lines coupled to the first source/drain region of at least one memory cell;

a number of bit lines coupled to the second source/drain region of at least one memory cell;

a number of wordlines coupled to the gate region of at least one memory cell;

a strapping line of lower resistance than the wordlines coupled to a single wordline wherein the strapping line bypasses a portion of the single wordline, and wherein the strapping line is spaced apart from adjacent conductive structures by a distance greater than a

wordline pitch[;], and wherein a width of the strapping line is greater than a width of the wordlines;

at least two channels connecting the strapping line to the single wordline; and

a system bus connecting the processing unit to the memory array.

30. (Twice amended) An information handling device comprising:

a processing unit;

at least one memory array comprising:

a number of memory cells having a first source/drain region and a second source/drain region and a gate region;

a number of source lines coupled to the first source/drain region of at least one memory cell;

a number of bit lines coupled to the second source/drain region of at least one memory cell;

an array of parallel wordlines coupled to the gate region of at least one memory cell, the array of parallel wordlines having a pitch;

a number of strapping devices which bypass portions of the wordlines in the array of parallel wordlines, each strapping device comprising:

a strapping line of lower resistance than the wordlines, wherein the strapping lines are each located a distance from each other that is greater than the pitch[;], and wherein a width of the strapping line is greater than a width of the wordlines; and

at least two channels connecting each strapping line to single wordlines; and

a system bus connecting the processing unit to the memory array.

37. (Twice amended) A method of reducing a wordline RC time constant comprising:

spacing a number of strapping devices over wordlines in a memory array apart from adjacent strapping devices by a distance greater than a wordline pitch[;], wherein a width of the strapping line is greater than a width of the wordlines; and

connecting individual strapping devices to portions of single wordlines using at least two channels for each strapping device;

activating a first number of transistors coupled to a first portion of a wordline; and

activating a second number of transistors coupled to a second portion of a wordline, wherein a signal used for activating the second number of transistors bypasses the first portion of the wordline through a strapping device of lower resistance than the first portion of the wordline;

activating a selected bitline in the memory array associated with a selected memory cell;

discharging the selected memory cell through a selected transistor, the selected transistor being activated by both the selected row and the selected bitline; and

sensing the presence or absence of a charge from the selected memory cell through the use of a sense amplifier.

42. (Twice amended) A method of reducing a wordline RC time constant in a memory bank comprising:

activating a plurality of selected coupled wordlines in a plurality of memory arrays, comprising:

activating a first wordline in a first memory array; and

activating a second wordline in a second memory array, wherein a signal used for activating the second wordline bypasses the first wordline through a strapping device of lower resistance than the first wordline, wherein the strapping device is spaced apart from adjacent strapping devices by a spacing greater than a wordline pitch, and <u>, wherein a width of the strapping device is greater than a width of the wordlines, and</u> wherein the strapping device is connected to the coupled wordlines by at least two channels;

activating a selected bitline in one of the plurality of memory arrays associated with a selected memory cell;

discharging the selected memory cell through a selected transistor, the selected transistor being activated by both the plurality of selected coupled wordlines and the selected bitline; and sensing the presence or absence of a charge from the selected memory cell through the use of a

sense amplifier.

45. (Twice amended) A method of forming a memory device comprising:

forming a number of memory cells having a first source/drain region and a second source/drain region and a gate region;

coupling a number of source lines to the first source/drain region of at least one memory cell;

coupling a number of bit lines to the second source/drain region of at least one memory cell;

attaching a number of wordlines to the gate region of at least one memory cell;

attaching a strapping line of lower resistance than the wordlines to a single wordline wherein the strapping line bypasses a portion of the single wordline, wherein the strapping line is spaced apart from adjacent conductive structures by a spacing greater than a wordline pitch[; and], and wherein a width of the strapping line is greater than a width of the wordlines; and

connecting the strapping line to the single wordline by forming at least two channels from the strapping line to the single wordline.

49. (Twice amended) A method of forming a memory device comprising:

forming a number of memory cells having a first source/drain region and a second source/drain region and a gate region;

coupling a number of source lines coupled to the first source/drain region of at least one memory cell;

coupling a number of bit lines coupled to the second source/drain region of at least one memory cell;

attaching an array of parallel wordlines to the gate region of at least one memory cell, the array of parallel wordlines having a pitch;

attaching a number of strapping lines of lower resistance than the wordlines which bypass portions of the wordlines in the array of parallel wordlines, wherein the strapping lines are each located a distance from each other that is greater than the pitch[; and], and wherein a width of the